Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1-10 (cancelled).

11 (currently amended): A chip-packaging with bonding options connected to a package substrate, comprising:

a package substrate;

a chip mounted on the package substrate, the chip comprising a plurality of bonding pads, a first bonding pad directly contacting the package substrate; ~~and~~

a first lead frame ~~directly contacting~~ connected to a second bonding pad through a first pin of the chip; and

a second lead frame connected to a third bonding pad through a second pin of the chip for receiving input signals to control the voltage level of the second pin.

12-18 (cancelled).

19 (currently amended): A method of packaging a chip having a bonding option connected to a package substrate, comprising:

providing the package substrate;

mounting the chip on the package substrate, the chip comprising a plurality of bonding pads;

connecting a first bonding pad directly to the package substrate; ~~and~~

connecting a second bonding pad ~~directly~~ to a first lead frame through a first pin of the chip;

connecting a third bonding pad to a second lead frame through a second pin of the chip; and

receiving input signals through the second lead frame for controlling the voltage level of the second pin.

20-26 (cancelled).

27 (new): A chip-packaging with bonding options connected to a package substrate, comprising:

a package substrate connected to either a high voltage or a low voltage;

a chip mounted on the package substrate, the chip comprising a plurality of bonding pads, a first bonding pad directly contacting the package substrate;

a first lead frame connected to a second bonding pad through a first pin of the chip, the first lead frame being connected to either a high voltage or a low voltage, and the voltage level of the first pin being the logical opposite of the voltage level of the package substrate; and

a second lead frame connected to a third bonding pad through a second pin of the chip for receiving input signals to control the voltage level of the second pin.

28 (new): The chip-packaging of claim 27, wherein the high voltage is a power supply and the low voltage is ground.

29 (new): The chip-packaging of claim 27, wherein the package substrate is connected to a power supply and the first lead frame is connected to ground.

30 (new): A method of packaging a chip having a bonding option connected to a package substrate, comprising:

providing the package substrate connected to either a high voltage or a low voltage;

mounting the chip on the package substrate, the chip comprising a plurality of bonding pads;

connecting a first bonding pad directly to the package substrate;

connecting a second bonding pad to a first lead frame through a first pin of the chip, the first lead frame being connected to either a high voltage or a low voltage, and the voltage level of the first pin being the logical opposite of the voltage level of the package substrate;

connecting a third bonding pad to a second lead frame through a second pin of the chip; and

receiving input signals through the second lead frame for controlling the voltage level of the second pin.

31 (new): The method of claim 30, wherein the high voltage is a power supply and the low voltage is ground.

32 (new): The method of claim 30, wherein the package substrate is connected to a power supply and the first lead frame is connected to ground.